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10/814,245	04/01/2004	Satoru Kojima	04329.3296	6964

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EXAMINER	
PATANKAR, ANEETA V	
ART UNIT	PAPER NUMBER
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/814,245	KOJIMA, SATORU	
	Examiner	Art Unit	
	Aneeta Patankar	2627	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *04/01/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. **Claim 1** is rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 6,278,724 B1 to *Zhou et al.*

As to **claim 1**, *Zhou* discloses a level detection circuit that detects a level change of a input value, comprising: a multiplication unit (106, 107) which multiplies the input value by a value (Fig. 26b, column 1-2, lines 59-17); an integration unit (108, 109) which integrates a result of multiplication by the multiplication unit (Fig. 26b, column 1-2, lines 59-17), where low-pass filter is the same as an integrator; and a comparison unit (110) which compares a result of integration by the integration unit with the input value, and detects a level change of the input value (Fig. 26b, column 1-2, lines 59-37), where the base band signals Ri and Rq are compared by the complex-type matched filter 110.

3. **Claim 4** is rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 7,376,056 B2 to *Nakao et al.*

As to **claim 4**, *Nakao* discloses a phase change detection circuit that detects a phase change of an input signal, comprising: a sine wave generating circuit (302) which generates, from the input signal, a reference sine wave having the same period as the input signal (Fig. 5, column 8-9, lines 52-20); a first integration unit (415) which multiplies the input signal by the reference sine wave, integrates a result of the multiplication, and provides a first integration result (Fig. 4, column 8-9, lines 52-24); a multiplication unit (409) which multiplies the first integration result by a value, and provides a multiplication result (Fig. 4, column 8-9, lines 52-24); a second integration unit (416) which integrates the multiplication result, and provides a second integration result (Fig. 4, column 8-9, lines 52-24); and a comparison unit (1111) which detects a level change of the first integration result as a phase change of the input signal by comparing the first integration result and the second integration result (Fig. 11, column 14-15, lines 18-10).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. **Claims 2 and 3** are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,278,724 B1 to *Zhou et al.* in view of U.S. Patent No. 5,307,084 to *Yamaguchi et al.*

As to **claim 2**, *Zhou* discloses a level detection circuit wherein the multiplication unit (51, 52, 53, 54) multiplies the input value by 1/a - b/c, wherein a, b, and c are arbitrary numbers (Fig. 6a, column 17, lines 42-45), and the integration unit (55) includes an adder unit (55) (Fig. 6a, column 18, lines 5-19), and the adder unit adding a result of multiplication by the multiplication unit (51, 52, 53, 54) and a result of computation by the arithmetic unit (Fig. 7a, columns 18-19, lines 38-6), where the entire circuit is an arithmetic unit for performing calculations on the input signals.

Zhou is deficient in disclosing an arithmetic unit which multiplies a result of addition by the adder unit by 1 - 1/a.

However, *Yamaguchi* discloses an arithmetic unit which multiplies a result of addition by the adder unit by 1 - 1/a (Fig. 1, column 3, lines 24-29). *Yamaguchi* is relied upon for his specific teaching of an arithmetic unit which multiples a result of addition by the added unit by 1-1/a, which can be directly applied to any arithmetic unit that has the same function of calculating changes in the input signals. Therefore, it would have been obvious to a person of ordinary skilled in the art to have created a level detection circuit where the integration unit includes an adder unit as taught by *Zhou* and an arithmetic unit with multiples a result of addition by another adder unit by 1-1/a as taught by *Yamaguchi*. The suggestion/motivation would have been in order to determine

the on/off state of the arithmetic circuit, or unit (Yamaguchi, column 4, lines 16-30)

As to **claim 3**, *Zhou* discloses a level detection circuit wherein the input value, a, b, and c are binary numbers, and the level detection circuit further comprises: a first bit adjustment unit which adjusts the number of bits of the input value input to the multiplication unit (Fig. 16, column 33, lines 4-22), where *Zhou* describes that the input signals can be converted into n-bit data; and a second bit adjustment unit which adjusts the number of bits of the result of integration such that the number of bits of the result of integration equals the number of bits of the input value when the result of integration and the input value are compared by the comparison unit (Fig. 17, columns 33-34, lines 63-21).

6. **Claim 7** is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 7,376,056 B2 to *Nakao et al.* in view of U.S. Patent No. 6,278,724 B1 to *Zhou et al*

As to **claim 7**, *Nakao* discloses an optical disk comprising: a wobble signal generating unit which generates a wobble signal from reflected light from a track on an optical disk on which a wobble, modulated using an address signal, is formed (Fig. 3, column 7, lines 36-47); a sine wave generating unit which generates from the wobble signal, a reference sine wave having the same period as the wobble signal (Fig. 3, column 7, lines 36-47); a first integration unit which multiplies the wobble signal by the reference sine wave, integrates a result of multiplication, and provides a first integration result (Fig. 4, column 8-9, lines 52-

24); an address extraction unit which extracts the address signal from the wobble signal in response to detection of the phase change (Fig. 4, column 8, lines 52-24), wherein the level detection unit comprises: a multiplication unit which multiplies the first integration result by a value, and provides a multiplication result (Fig. 4, column 8-9, lines 52-24); a second integration unit which integrates the multiplication result, and provides a second integration result (Fig. 4, column 8-9, lines 52-24); and a comparison unit which compares the first integration result and the second integration result, and detects a signal level change of the first integration result (Fig. 11, column 14-15, lines 18-10).

Nakao is deficient in disclosing a level detection unit which detects a level change of the first integration result as a phase change of the wobble signal.

However, *Zhou* discloses a level detection unit which detects a level change of the first integration result as a phase change of the wobble signal (Fig. 26b, column 1-2, lines 59-17).

Zhou is relied upon for his specific teaching of a circuit having a feature that detects a level change of an integration result, which can be directly applied to any circuit that has the same function of detecting a phase change in a signal. Therefore, it would have been obvious to a person of ordinary skilled in the art to have created a wobble signal generating unit as taught by *Nakao* and a level detection unit as taught by *Zhou*. The suggestion/motivation would have been in order to filter out pseudo noise (Zhou, Fig. 26b, column 2, lines 18-37).

7. **Claims 5, 6, 8 and 9** are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 7,376,056 B2 to *Nakao et al.* in view of U.S. Patent No. 6,278,724 B1 to *Zhou et al.* and in further view of U.S. Patent No. 5,307,084 to *Yamaguchi et al.*

As to **claim 5**, *Nakao* is deficient in disclosing a phase change detection circuit, wherein the multiplication unit multiplies the input value by 1/a - b/c where a, b, and c are arbitrary numbers, the second integration unit includes an adder unit, and an arithmetic unit which multiplies a result of addition by the adder unit by 1 - 1/a, and the adder unit adds the multiplication result provided by the multiplication unit and a result of computation by the arithmetic unit.

However, *Zhou* discloses a phase change detection circuit, wherein the multiplication unit multiplies the input value by 1/a - b/c where a, b, and c are arbitrary numbers (column 13, lines 43-68), the second integration unit includes an adder unit, and the adder unit adds the multiplication result provided by the multiplication unit and a result of computation by the arithmetic unit (Fig. 6a, column 17-18, lines 5-19).

At the time of invention, it would have been obvious to a person of ordinary skilled in the art to have created a wobble signal generating unit as taught by *Nakao* and a level detection unit as taught by *Zhou*. The suggestion/motivation would have been in order to filter out pseudo noise (*Zhou*, Fig. 26b, column 2, lines 18-37).

Furthermore, *Yamaguchi* discloses an arithmetic unit which multiplies a result of addition by the adder unit by 1 - 1/a (Fig. 1, column 3, lines 9-48).

Yamaguchi is relied upon for his specific teaching of a circuit having an arithmetic unit which multiples a result of addition by the added unit by 1-1/a which can be directly applied to any circuit that has the same function of calculating an output signal based on input signals into a circuit. Therefore, it would have been obvious to a person of ordinary skilled in the art to have created a sine wave generating circuit as taught by *Nakao* and an arithmetic unit as taught by *Yamaguchi*. The suggestion/motivation would have been in order to determine the on/off state of the arithmetic circuit, or unit (Yamaguchi, column 4, lines 16-30).

As to **claim 6**, *Nakao* is deficient in disclosing a phase change detection circuit wherein the input value, a, b, and c are binary numbers, and the phase change detection circuit further comprises: a first bit adjustment unit which adjusts the number of bits of the input value input to the multiplication unit; and a second bit adjustment unit which adjusts the number of bits of the second integration result such that the number of bits of the second integration result equals the number of bits of the input value when the second integration result and the input value are compared by the comparison unit.

However, *Zhou* discloses a phase change detection circuit wherein the input value, a, b, and c are binary numbers, and the phase change detection circuit further comprises: a first bit adjustment unit which adjusts the number of bits of the input value input to the multiplication unit (Fig. 16, column 33, lines 4-22), where *Zhou* describes that the input signals can be converted into n-bit data;

and a second bit adjustment unit which adjusts the number of bits of the second integration result such that the number of bits of the second integration result equals the number of bits of the input value when the second integration result and the input value are compared by the comparison unit (Fig. 17, column 33-34, lines 63-21). In addition, the same motivation is used as the rejection in claim 5.

As to **claim 8**, *Nakao* is deficient in disclosing an optical disk wherein the multiplication unit multiplies the input value by 1/a - b/c, wherein a, b, and c are arbitrary numbers, and the integration unit includes an adder unit, and an arithmetic unit which multiplies a result of addition by the adder unit by 1-1/a, the adder unit adding the multiplication result provided by the multiplication unit and a result of computation by the arithmetic unit.

However, *Zhou* discloses an optical disk wherein the multiplication unit multiplies the input value by 1/a - b/c, wherein a, b, and c are arbitrary numbers (column 13, lines 43-68), and the integration unit includes an adder unit (Fig. 6a, column 17-18, lines 5-19), the adder unit adding the multiplication result provided by the multiplication unit and a result of computation by the arithmetic unit (Fig. 6a, column 17-18, lines 5-19).

At the time of invention, it would have been obvious to a person of ordinary skilled in the art to have created a wobble signal generating unit as taught by *Nakao* and a level detection unit as taught by *Zhou*. The suggestion/motivation would have been in order to filter out pseudo noise (*Zhou*, Fig. 26b, column 2, lines 18-37).

Furthermore, *Yamaguchi* discloses an arithmetic unit which multiplies a result of addition by the adder unit by 1-1/a (Fig. 1, column 3, lines 9-48). In addition, the same motivation is used as the rejection for claim 5.-

As to **claim 9**, *Nakao* is deficient in disclosing an optical disk apparatus, wherein the input value, a, b, and c are binary numbers, and the phase change detection circuit further comprises: a first bit adjustment unit which adjusts the number of bits of the input value input to the multiplication unit; and a second bit adjustment unit which adjusts the number of bits of the second integration result such that the number of bits of the second integration result equals the number of bits of the input value when the second integration result and the input value are compared by the comparison unit.

However, *Zhou* discloses an optical disk apparatus, wherein the input value, a, b, and c are binary numbers, and the phase change detection circuit further comprises: a first bit adjustment unit which adjusts the number of bits of the input value input to the multiplication unit (Fig. 16, column 33, lines 4-22); and a second bit adjustment unit which adjusts the number of bits of the second integration result such that the number of bits of the second integration result equals the number of bits of the input value when the second integration result and the input value are compared by the comparison unit (Fig. 17, column 33-34, lines 63-21). In addition, the same motivation is used as the rejection in claim 5.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aneeta Patankar whose telephone number is (571) 272-9773. The examiner can normally be reached on Monday-Thursday 8-5, Second Friday, 8-4.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Andrea Wellington can be reached on (571) 272-4483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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